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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/877,232	06/11/2001	Shinji Ozaki	60188-077	8544

7590 01/12/2004

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EXAMINER	
TORRES, JOSEPH D	

ART UNIT	PAPER NUMBER
2133	6

DATE MAILED: 01/12/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/877,232	OZAKI, SHINJI	
	Examiner	Art Unit	
	Joseph D. Torres	2133	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *11 June 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-10* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-10* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *11 June 2001* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. §§ 119 and 120

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

13)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application) since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

a) ☐ The translation of the foreign language provisional application has been received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121 since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *4* .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Drawings

1. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they include the following reference sign(s) not mentioned in the description: '34' in Figure 4. A proposed drawing correction, corrected drawings, or amendment to the specification to add the reference sign(s) in the description, are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

2. Claims 1, 4 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hsu, Rong-Fu (US 5938774 A).

35 U.S.C. 103(a) rejection of claim 1.

Hsu teaches a circuit for modifying output data of storage (see Abstract Hsu; Note: a circuit apparatus for repairing faulty program segments is a circuit for modifying output data of storage) means, the storage means outputting a data segment (ROM 60 is a storage means outputting a data word), the data segments being stored at respective addresses, the address or location of each segment being specified by a starting address on the storage means (Storage Table 60 in Figure 3B teaches that each segment in the storage device is defined by its starting address, see col. 5, lines 37-45, Hsu), the circuit comprising: a data register for retaining correction data with the width of each segment (RAM unit 70 in Figure 3B teaches a storage means for retaining correction data with the width of each segment; Note: replacing the RAM unit 70 of Figure 3B with a register does not deviate from the scope or the intent of the teachings in the Hsu patent since a register is still a storage means) thereon; an address register for retaining a correction address (see Faulty Segment Address Table 10 in Figures 2 and 3A of Hsu; Note: replacing the Faulty Segment Address Table 10 of Figures 2 and 3A with a register does not deviate from the scope or the intent of the teachings in the Hsu patent since a register is still a storage means) thereon; a correspondence detector, which receives the address signal and the correction address and determines whether or not correspondence is found between the correction address and one of a number of addresses starting at, or preceding, the address specified by the address signal (the abstract in Hsu teaches when the current access address corresponds to the

starting address of any one of the faulty program segments , a comparison circuit and a multiplexer are used in conjunction to change the access address to the starting address of the corresponding repair program segment in the RAM unit, hence the comparison circuit 20 and the multiplexer 50 in Figure 2 of Hsu are a correspondence detector, which receives the current access address signal from Program Counter 40 in Figure 3A and the correction address from Faulty Segment Address Table 10 of Figures 2 and 3A and determines whether or not correspondence is found between the correction address from Faulty Segment Address Table 10 of Figures 2 and 3A and one of a number of program access addresses from Program Counter 40 in Figure 3A starting at, or preceding, the address specified by the address signal, Note: one of a number of addresses starting at, or preceding, the address specified by the address signal implies that any one of the address in the range are used and the current program access address is certainly an address within that specified range); and a stored data selecting section for selectively outputting, on a byte-by-byte basis, either the output data of the storage means or the correction data in accordance with the address signal and the correction address if the correspondence detector has found the correspondence, wherein the circuit delivers the output of the stored data selecting section as modified stored data (MUX 50 in Figure 3A either selects the current program access address signal or the corresponding correction address used to determine the actual modified output of ROM/RAM unit 60 and 70 in Figure 2 in Hsu; Note: a specific byte-by-byte means for outputting does not deviate from the scope or

the intent of the teachings in the Hsu patent since the Hsu patent requires an output means for the ROM/RAM unit).

However Hsu, does not explicitly teach the specific use of the segments taught in the Hsu patent are data word with a width of 2^N bytes where N is a natural number, (Note: a word is a row in a memory array module or modules, read out a unit at a time specified by its row address which starts at an address specified as a multiple of 2^N by an address signal since the first element of a row in memory always has the column address 000...0; Note also in a 2^N x2^N memory only 2^N row addresses are required to specify all of the addresses).

The Examiner would like to point out that it would have been obvious to use a specific embodiment of the Hsu patent whereby the segment length is restricted to the word width of an 2^N x2^N memory array unit. One of ordinary skill in the art at the time the invention was made would have been highly motivated to restrict the segment length to the word width of an 2^N x2^N memory array unit in order to maintain consistency with bus technologies since in current bus technologies data is read out in bursts or widths of 2^N. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the teachings of Hsu by including an additional step of restricting the segments taught in the Hsu patent to data word with a width of 2^N bytes where N is a natural number. This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that restricting the segments taught in the Hsu patent to data word with a width of 2^N bytes where N is a natural number would have provided

the opportunity to maintain consistency with bus technologies since in current bus technologies data is read out in bursts or widths of 2^N.

35 U.S.C. 103(a) rejection of claim 4.

Hsu, substantially teaches the claimed invention described in claim 1 (as rejected above).

However Hsu does not explicitly teach the specific use of a specific means for outputting data after selection.

The Examiner asserts that a specific byte-by-byte means for outputting does not deviate from the scope or the intent of the teachings in the Hsu patent since the Hsu patent requires an output means for the ROM/RAM unit and a specific byte-by-byte means for outputting is a specific embodiment of the teachings in Hsu used to implement the required outputting means in the Hsu patent.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the teachings of Hsu by including use of a specific means for outputting data after selection. This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that use of a specific means for outputting data after selection would have provided the opportunity to implement the required outputting means in the Hsu patent.

35 U.S.C. 103(a) rejection of claim 5.

Hsu, substantially teaches the claimed invention described in claim 1 (as rejected above).

However Hsu does not explicitly teach the specific use of a specific means for detecting correspondence.

The Examiner asserts that a specific means for detecting correspondence does not deviate from the scope or the intent of the teachings in the Hsu patent since the Hsu patent requires a correspondence detecting means and a specific means for detecting correspondence is a specific embodiment of the teachings in Hsu used to implement the required correspondence detecting means in the Hsu patent.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the teachings of Hsu by including use of a specific means for detecting correspondence. This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that use of a specific means for detecting correspondence would have provided the opportunity to implement the required correspondence detecting means in the Hsu patent.

35 U.S.C. 103(a) rejection of claim 6.

Hsu teaches a circuit for modifying output data of storage (see Abstract Hsu; Note: a circuit apparatus for repairing faulty program segments is a circuit for modifying output data of storage) means, the storage means outputting a data segment (ROM 60 is a storage means outputting a data word), the data segments being stored at respective

addresses, the address or location of each segment being specified by a starting address on the storage means (Storage Table 60 in Figure 3B teaches that each segment in the storage device is defined by its starting address, see col. 5, lines 37-45, Hsu), the circuit comprising: a number of data registers, each said data register retaining correction data with the width of 2.sup.N bytes thereon (RAM unit 70 in Figure 3B teaches a storage means for retaining correction data with the width of each segment; Note: replacing the RAM unit 70 of Figure 3B with a number of data registers does not deviate from the scope or the intent of the teachings in the Hsu patent since a number of data registers is still a storage means) thereon; the same number of address registers, each said address register retaining a correction address thereon, the data and address registers forming the same number of register pairs (see Faulty Segment Address Table 10 in Figures 2 and 3A of Hsu; Note: replacing the Faulty Segment Address Table 10 of Figures 2 and 3A with the same number of address registers, whereby said address register retains a correction address thereon, the data and address registers forming the same number of register pairs does not deviate from the scope or the intent of the teachings in the Hsu patent since a number of address registers is still a storage means and the address storage means in the Hsu patent requires the same number of address registers, whereby said address register retains a correction address thereon, the data and address registers forming the same number of register pairs) thereon; the same number of correspondence detectors, each said correspondence detector being associated with one of the register pairs and determining, responsive to the address signal and the correction address retained on

the associated address register, whether or not correspondence is found between the correction address and one of a number 2^N of addresses starting at the address specified by the address signal or between the correction address and one of a number (2^{N-1}) of addresses preceding the address specified by the address signal (the abstract in Hsu teaches when the current access address corresponds to the starting address of any one of the faulty program segments, a comparison circuit and a multiplexer are used in conjunction to change the access address to the starting address of the corresponding repair program segment in the RAM unit, hence the comparison circuit 20 and the multiplexer 50 in Figure 2 of Hsu are a correspondence detector, which receives the current access address signal from Program Counter 40 in Figure 3A and the correction address from Faulty Segment Address Table 10 of Figures 2 and 3A and determines whether or not correspondence is found between the correction address from Faulty Segment Address Table 10 of Figures 2 and 3A and one of a number of program access addresses from Program Counter 40 in Figure 3A starting at, or preceding, the address specified by the address signal, Note: one of a number of addresses starting at, or preceding, the address specified by the address signal implies that any one of the address in the range are used and the current program access address is certainly an address within that specified range; Note also that Figure 3A in Hsu breaks the comparators into a same number of correspondence detectors, each said correspondence detector being associated with one of the register pairs and determining, responsive to the address signal and the correction address retained on the associated address register, whether or not correspondence is found between the

correction address); and a data register selector, which receives the outputs of the correspondence detectors and outputs, as selected correction data, the correction data retained on one of the data registers that is associated with one of the correspondence detectors that has found the correspondence; an address register selector, which also receives the outputs of the correspondence detectors and outputs, as a selected correction address, the correction address retained on one of the address registers that is associated with the correspondence detector that has found the correspondence; and a stored data selecting section for selectively outputting, on a byte-by-byte basis, either the output data of the storage means or the selected correction data, output from the data register selector, in accordance with the address signal and the selected correction address, output from the address register selector, if the correspondence detector has found the correspondence, wherein the circuit delivers the output of the stored data selecting section as modified stored data (MUX 50 in Figure 3A either selects the current program access address signal or the corresponding correction address used to determine the actual modified output of ROM/RAM unit 60 and 70 in Figure 2 in Hsu; Note: a specific byte-by-byte means for outputting does not deviate from the scope or the intent of the teachings in the Hsu patent since the Hsu patent requires an output means for the ROM/RAM unit).

However Hsu, does not explicitly teach the specific use of the segments taught in the Hsu patent are data word with a width of 2^N bytes where N is a natural number, (Note: a word is a row in a memory array element or elements read out a unit at a time specified by its row address which starts at an address specified as a multiple of 2^N by an

address signal since the first element of a row in memory always has the column address 000...0; Note also in a 2^N x2^N memory only 2^N row addresses are required to specify all of the addresses).

The Examiner would like to point out that it would have been obvious to use a specific embodiment of the Hsu patent whereby the segment length is restricted to the word width of an 2^N x2^N memory array unit. One of ordinary skill in the art at the time the invention was made would have been highly motivated to restrict the segment length to the word width of an 2^N x2^N memory array unit in order to maintain consistency with bus technologies since in current bus technologies data is read out in bursts or widths of 2^N. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the teachings of Hsu by including an additional step of restricting the segments taught in the Hsu patent to data word with a width of 2^N bytes where N is a natural number. This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that restricting the segments taught in the Hsu patent to data word with a width of 2^N bytes where N is a natural number would have provided the opportunity to maintain consistency with bus technologies since in current bus technologies data is read out in bursts or widths of 2^N.

35 U.S.C. 103(a) rejection of claim 9.

Hsu, substantially teaches the claimed invention described in claim 1 (as rejected above).

However Hsu does not explicitly teach the specific use of a specific means for outputting data after selection.

The Examiner asserts that a specific byte-by-byte means for outputting does not deviate from the scope or the intent of the teachings in the Hsu patent since the Hsu patent requires an output means for the ROM/RAM unit and a specific byte-by-byte means for outputting is a specific embodiment of the teachings in Hsu used to implement the required outputting means in the Hsu patent.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the teachings of Hsu by including use of a specific means for outputting data after selection. This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that use of a specific means for outputting data after selection would have provided the opportunity to implement the required outputting means in the Hsu patent.

35 U.S.C. 103(a) rejection of claim 10.

Hsu, substantially teaches the claimed invention described in claim 1 (as rejected above).

However Hsu does not explicitly teach the specific use of a specific means for detecting correspondence.

The Examiner asserts that a specific means for detecting correspondence does not deviate from the scope or the intent of the teachings in the Hsu patent since the Hsu

patent requires a correspondence detecting means and a specific means for detecting correspondence is a specific embodiment of the teachings in Hsu used to implement the required correspondence detecting means in the Hsu patent.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the teachings of Hsu by including use of a specific means for detecting correspondence. This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that use of a specific means for detecting correspondence would have provided the opportunity to implement the required correspondence detecting means in the Hsu patent.

Allowable Subject Matter

3. Claims 2, 3, 7 and 8 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The following is an Examiner's statement of reasons for the indication of allowable subject matter:

The present invention pertains to a method for modifying output data of storage means. Claim 2 recites: "a byte selection controller for controlling the selective output of the byte selector in accordance with an N^{th}-bit value of the address signal, a low-order-(N+1)-bit

value of the selected correction address output from the address register selector and the outputs of the correspondence detectors".

The Prior Art of record and, in particular, Hsu teach a method for modifying output data of storage (see Abstract Hsu; Note: a circuit apparatus for repairing faulty program segments is a circuit for modifying output data of storage) means, the storage means outputting a data segment (ROM 60 is a storage means outputting a data word), the data segments being stored at respective addresses, the address or location of each segment being specified by a starting address on the storage means (Storage Table 60 in Figure 3B teaches that each segment in the storage device is defined by its starting address, see col. 5, lines 37-45, Hsu), the circuit comprising: a data register for retaining correction data with the width of each segment (RAM unit 70 in Figure 3B teaches a storage means for retaining correction data with the width of each segment; Note: replacing the RAM unit 70 of Figure 3B with a register does not deviate from the scope or the intent of the teachings in the Hsu patent since a register is still a storage means) thereon; an address register for retaining a correction address (see Faulty Segment Address Table 10 in Figures 2 and 3A of Hsu; Note: replacing the Faulty Segment Address Table 10 of Figures 2 and 3A with a register does not deviate from the scope or the intent of the teachings in the Hsu patent since a register is still a storage means) thereon; a correspondence detector, which receives the address signal and the correction address and determines whether or not correspondence is found between the correction address and one of a number of addresses starting at, or preceding, the address specified by the address signal (the abstract in Hsu teaches when the current

access address corresponds to the starting address of any one of the faulty program segments , a comparison circuit and a multiplexer are used in conjunction to change the access address to the starting address of the corresponding repair program segment in the RAM unit, hence the comparison circuit 20 and the multiplexer 50 in Figure 2 of Hsu are a correspondence detector, which receives the current access address signal from Program Counter 40 in Figure 3A and the correction address from Faulty Segment Address Table 10 of Figures 2 and 3A and determines whether or not correspondence is found between the correction address from Faulty Segment Address Table 10 of Figures 2 and 3A and one of a number of program access addresses from Program Counter 40 in Figure 3A starting at, or preceding, the address specified by the address signal, Note: one of a number of addresses starting at, or preceding, the address specified by the address signal implies that any one of the address in the range are used ant the current program access address is certainly an address within that specified range); and a stored data selecting section for selectively outputting, on a byte-by-byte basis, either the output data of the storage means or the correction data in accordance with the address signal and the correction address if the correspondence detector has found the correspondence, wherein the circuit delivers the output of the stored data selecting section as modified stored data (MUX 50 in Figure 3A either selects the current program access address signal or the corresponding correction address used to determine the actual modified output of ROM/RAM unit 60 and 70 in Figure 2 in Hsu; Note: a specific byte-by-byte means for outputting does not deviate

from the scope or the intent of the teachings in the Hsu patent since the Hsu patent requires an output means for the ROM/RAM unit).

The prior art however are not concerned with and do not teach a method step for a byte selection controller for controlling the selective output of the byte selector in accordance with an N^{th}-bit value of the address signal, a low-order-(N+1)-bit value of the selected correction address output from the address register selector and the outputs of the correspondence detectors as taught by claim 2 and its base and intervening claims. Hence the prior art taken alone or in any combination fail to teach the claimed novel feature in claim 2 in view of its base and intervening claims.

Claim 3 depends from claim 2 and is allowable for the same reasons as claim 2.

Claims 7 recites substantially similar language as in claim 2.

Claim 8 depends from claim 7 and is allowable for the same reasons as claim 7.

Conclusion

4. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Matsuura, Tsuguo et al. (US 4385351 A) teaches a data processing system of the multi-processor type, having a plurality of central processing units. Olson, Stephen W. et al. (US 5377338 A) teaches methods and apparatus for interfacing a central processor and an IO controller to a main memory. Sakai, Kikuo (US 4780875 A) teaches memory access for memory arrays. Kennedy, Barry (US 5301281 A) teaches memory access for memory arrays.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Joseph D. Torres whose telephone number is (703) 308-7066. The examiner can normally be reached on M-F 8-5.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert Decady can be reached on (703) 305-9595. The fax phone number for the organization where this application or proceeding is assigned is (703) 746-7239.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703)-746-7240.

Joseph D. Torres, PhD
Art Unit 2133